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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/735,993	12/12/2000	Shuzo Kato	252/008	5072

22850 7590 03/28/2005

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EXAMINER	
ZHENG, EVA Y	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/735,993	KATO ET AL.	
	Examiner	Art Unit	
	Eva Yi Zheng	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,9-15,17-23* is/are rejected.

7)☒ Claim(s) *2,3,8 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed October 8, 2004 have been fully considered but they are not persuasive. The Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

a) Applicant's argument – Claim 1, Park et al. doe not disclose or suggest claimed "inphase register" and "quadrature register" as the present application.

Examiner's response – Park et al. disclose a digital predistortion technique in a communication system. According to Park et al, a typical predistortion technique comprises input data coupled to shift register (11 in Fig. 1) and input to a ROM (13 in Fig. 1), which generate I and Q signal (Col 3, L35- Col 4, L44). Both shift register and ROM by Park et al. constitute claimed "inphase register" and "quadrature register" as the present application.

b) Applicant's argument – Park do not disclose or suggest Applicants' claim of "the modified inphase and quadrature analog data replaces the inphase and quadrature analog signals at the output of the DACs".

Examiner's response – In Fig. 7 of Park et al. the predistortion coefficients IPDD and QPDD are converted by DAC 237. The outputs of DAC 237 are constitute as claimed "modified inphase and quadrature analog data". The multiplier 511 and 513 correlating the output of DAC 205 and 207 with DAC 237 and generating predistorted I and Q channel signal, respectively. Since the output is no longer the same as the output

of DACs (205 and 207), Park et al. did not fail to teach claimed, "replaces the inphase and quadrature analog signals at the output of the DACs". Applicant is reminded that the Examiner is entitled to give the broadest reasonable interpretation to the language of claims.

c) Applicant's argument – Claim 14, Park did not teach EVM scatter pattern.

Examiner's response – Park et al. disclose multiplying the input baseband data IchD and QchD by the predistortion data IPDD and QPDD, respectively. The distortion characteristics are measured in advance and stored in the predistortion lookup tables in the memory 233 (Col 10, L51-68). Those skill in the art will realize that I and Q data are mapped as constellation point representing scatter patterns in presdistortion system. Therefore, I and Q signals constitute as known EVM scatter patterns.

d) Applicant's argument – Claim 20, Park did not teach Applicants' claimed step of testing and there is no mention of "overshoot" and "error vector magnitude scatter patterns".

Examiner's response – Park et al. disclose a digital predistortion technique in a communication system. A temperature sensor (229 in Fig. 7) senses the surrounding temperature of the transmitter and provides the address former (231) with the temperature sensing signal and store predistorting baseband data in a lookup table (Col 12, L 50-67). All these inherent as "testing the detect overshoot". "Overshoot" by definition is caused by distortion of signals. Although Park et al. did not explicitly mention word "overshoot", those skill in the art will realize predistortion technique by Park et al. is equivalent as "overshoot" by applicant. Park et al. also disclose error

vector magnitude scatter pattern with similar reasons as mentioned in the Examiner's response above.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4, 6, 7, 9, 10, 12, 14, 15, 17, 18, and 20, 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. (US 6,373,902 B1).

a) Regarding claims 1, 9, 15, 17, and 21, Park et al. disclose a predetermined error vector magnitude reduction circuit comprising:

an inphase register for storing digital inphase bit patterns (11 and 13 in Fig. 1);

a quadrature register for storing digital quadrature bit patterns (11 and 13 in Fig. 1);

an inphase digital-to-analog converter (DAC) for converting the digital inphase bit patterns to an inphase analog signal (205 in Fig. 7);

a quadrature DAC for converting the digital quadrature bit patterns to a quadrature analog signal (207 in Fig. 7); and

at least one lookup table (233 in Fig. 7) containing predetermined digital inphase and quadrature bit patterns for comparison with the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers, and containing modified inphase and quadrature analog data that do not cause overshoot, wherein the modified inphase and quadrature analog data replaces the inphase and quadrature analog signals at the output of the DACs when there is a match between the predetermined digital inphase and quadrature bit patterns stored in the lookup table and the digital inphase and quadrature bit patterns stored in the inphase and quadrature registers (Col 5, L 22-35).

b) Regarding claims 4, 6, 10 and 12, Park et al. disclose the circuit further comprising a storage element for storing the lookup table (233 in Fig. 7; Col 5, L 22-35).

c) Regarding claims 5 and 11, Park et al. disclose wherein the storage element is one of a group comprised of a SRAM, a DRAM, an EPRON, an EEPROM< and a Flash (21 in Fig. 1).

d) Regarding claim 7, Park et al. disclose the circuit of claim 1, further comprising an adder for adding the inphase and quadrature analog signals (213 in Fig. 7).

e) Regarding claim 14, Park et al. disclose a transmitter comprising:

a baseband processor for generating inphase and quadrature digital bit patterns ("IchD" and "QchD" as shown in Fig. 7);

a predetermined error vector magnitude (EVM) reduction circuit for converting the inphase and quadrature digital bit patterns to analog signals that minimize EVM

by correlating the inphase and quadrature digital bit patterns to known EVM scatter patterns (201, 203, 205, 207, 511, 513, 209, 211, 229, 231, 233, and 237 in Fig. 7);

a mixing stage for mixing the analog signal up to an RF signal (213 in Fig. 7);

a power amplifier for amplifying the RF signal (217 in Fig. 7); and

an antenna for transmitting the RIF signal (225 in Fig. 7).

f) Regarding claim 13, Park et al. disclose the circuit of claim 9, wherein the lookup table is implemented in software (21 in Fig. 1).

g) Regarding claim 18, Park et al. disclose the transmitter of claim 14, wherein the mixing stage comprises a first mixer (213 in Fig. 7) for mixing the analog signal to an intermediate frequency, followed by a second mixer (219 in Fig. 7) wherein the intermediate frequency signal is mixed with an RF carrier to create an RF signal (Col 13, L49-60).

h) Regarding claim 19, Park et al. disclose the transmitter of claim 14, wherein the transmitter is included in a handset that is part of a system from a group comprised of a wireless communication system, a cordless telephone system, a wireless local loop, and a satellite communications system (inherent as a digital radio communication system; abstract).

i) Regarding claim 20, Park et al. disclose a method for predetermined error vector magnitude reduction comprising the following steps:

testing to detect overshoot in transitions from one phase state to another at the output of a transmitter (as shown in Fig. 7);

correlating the overshoot to particular error vector magnitude scatter patterns (511 and 513 in Fig. 7);

correlating the scatter patterns to particular inphase and quadrature bit patterns (511 and 513 in Fig. 7);

forming a lookup table containing the predetermined inphase and quadrature bit patterns and modified inphase and quadrature data for each of the bit patterns that does not cause overshoot (233 in Fig. 7; Col 5, L 22-35); and

using the lookup table to prevent or reduce error vector magnitude at the output of the transmitter (Col 5, L 22-35).

j) Regarding claim 22, Park et al. disclose the method of claim 20, wherein the modified inphase and quadrature data is digital data (201 and 203 in Fig. 7).

k) Regarding claim 23, Park et al. disclose the method of claim 20, wherein the modified inphase and quadrature data is analog data (205 and 207 in Fig. 7).

Allowable Subject Matter

4. Claims 2, 3, 8 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Yi Zheng whose telephone number is (571) 272-3049. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-879-9306.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Eva Yi Zheng
Examiner
Art Unit 2634

March 14, 2005

SHUWANG LIU
PRIMARY EXAMINER